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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,084	03/31/2004	Maged M. Ghoneima	INTEL-0065	5661
34610	7590	05/02/2005	EXAMINER	
FLESHNER & KIM, LLP P.O. BOX 221200 CHANTILLY, VA 20153			WILLIAMS, HOWARD L	
		ART UNIT	PAPER NUMBER	
		2819		
DATE MAILED: 05/02/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,084	GHONEIMA ET AL.	
	Examiner	Art Unit	
	Howard L. Williams	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on _____.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 1-9 and 16-18 is/are allowed.

6) Claim(s) 10-15 and 19-21 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 033104.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-21 are rejected under 35 U.S.C. 102(e) as anticipated by Lin Li et al.

article A *Crosstalk Aware Interconnect with Variable Cycle Transmission*.

Li discloses in figure 7 a DYN + Bus Invert technique which either passes the data unchanged or selects the coding block via the mux for bus invert coding. Memory element for the input data is read upon the first latch (left side of figure 7) and flip-flops for delay insertion as the second set of latches coupled to the mux output. The “DYN”

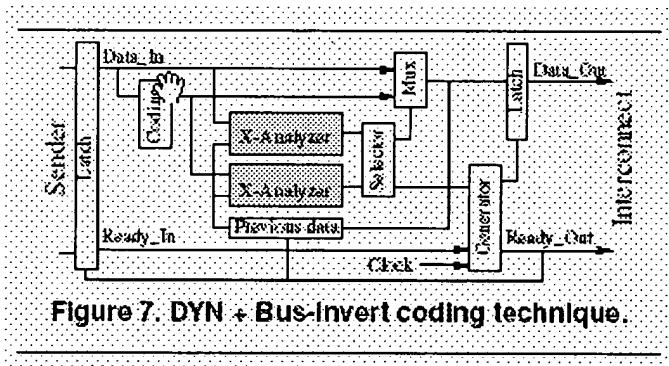


Figure 7. DYN + Bus-Invert coding technique.

or dynamic portion of the technique is described on page 2 left hand column first bullet where the method of analyzing the data to determine dynamically the number of clock cycles for transmission.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin Li et al. article in view of US 5632029 A to Bruce et al. Lin Li et al. discloses a bus interconnect architecture with bus invert coding and dynamic data based delayed as set forth above. Lin Li et al. does not disclose the bus as multi-segmented or multi-stage. Bruce et al. discloses (col. 1, lines 28-67) the use of multi-segment bus for communication among the various chips and IC boards to increase bandwidth and avoid long runs. It would have been obvious to combine the Lin Li interconnect architecture with the multi-segment bus of Bruce to further improve the bandwidth, reduce power consumption and bus noise.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5337252 A to Lac et al. discloses a connector/pin pattern arrangement to provide "delta-I noise minimization" in which like conductors are not assigned adjacent locations. US 5689258 A to Nakamura et al. discloses the reduction of inverter delay with increased supply voltages. US 5763908 A to Han et al. discloses a grouping of adjacent conductors and their connection to first or second voltages based on their group. US 6708314 B2 to Trivedi discloses the use of shield wires at different power levels on either side of bus wiring. US 20030025122 A1 to Nakamura et

al. alternating read/write wires adjacent to one another are powered at different levels during the respective read/write cycles to serve as shield wires for their adjacent conductors.

Claims 1-9 and 16-18 are allowed over the art of record. The art of record was not seen to disclose the provision of adjacent and parallel drivers for the interconnects being powered by different voltages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard L. Williams at telephone number (571) 272-1815.

4/27/05
Voice: (571) 272-1815

Howard L. Williams
Howard L. Williams
Primary Examiner
Art Unit 2819